LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A decision directed phase locked loop circuit, comprising:

a phase detector which receives an input sequence of baseband complex samples in a burst data communication system and current phase estimates and generates phase differences between said baseband complex samples and current phase estimates;

an inner block decoder which decodes said baseband complex samples to generate decoded data;

a phase error generation circuit which receives said baseband complex samples and said decoded data from said inner block decoder and which generates feedback phase error terms based on said baseband complex samples and said decoded data, wherein said inner block decoder and phase error generation circuit are adapted to selectively apply excess processing power to a burst in said burst data communication system;

a selection circuit which identifies a burst to be demodulated with excess processing power, said selection circuit providing said identified burst to said inner block decoder and said phase error generation circuit so as to selectively apply excess processing power in order to re-process said burst;

an outer block decoder which receives the associated codewords generated by said inner block decoder and which utilizes and corrects only codewords associated with baseband complex samples after the group of baseband complex samples consisting of the first baseband complex samples received by said phase detector;

a loop filter which filters said phase error terms; and

a phase accumulator that updates the current phase estimate on each iteration of the phase locked loop.

2. (Original) A decision directed phase locked loop as claimed in claim 1, wherein the baseband complex samples are demodulated from an input modulated signal corresponding to one of a binary phase shift keying (BPSK) modulated signal and a quaternary phase shift keying (QPSK) modulated signal and encoded by a sequence of codewords.

3. (Original) A decision directed phase locked loop as claimed in claim 2, wherein said codewords correspond to biorthogonal binary codes.

4. (Original) A decision directed phase locked loop as claimed in claim 3, wherein each of said codewords contains four data symbols, and the decode rate for decoding a set of vector pairs of phase stabilized observables corresponds to one quarter of a symbol rate.

5. (Original) A decision directed phase locked loop as claimed in claim 4, wherein said inner block decoder comprises a Reed-Muller block decoder.

6. (Original) A decision directed phase locked loop as claimed in claim 5, wherein said phase error generation circuit generates said feedback phase error terms based on the composite decoded codeword phase error relative to reference.

7. (Original) A decision directed phase locked loop as claimed in claim 6, wherein said current phase estimate is updated at one quarter the symbol rate.

8. (Original) A decision directed phase locked loop as claimed in claim 6, wherein said current phase estimate is updated every codeword of four data symbols.

9. (Original) A decision directed phase locked loop as claimed in claim 1, wherein said phase detector includes a subtractor for subtracting the incoming phase of said baseband complex samples from the current phase estimate to generate said phase differences.

10. (Currently Amended) A demodulator for demodulating an input modulated signal in a burst data communications system, comprising:

a plurality of phase locked loops, each having a first block decoder configured to decode bursts of the input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate, wherein one of said plurality of phase locked loops is adapted to selectively apply excess processing power to a burst of said input modulated signal; and

a selection circuit which identifies [[a]] the burst of said input modulated signal to be demodulated with excess processing power, said selection circuit providing said identified burst to said one of said plurality of phase locked loops which is adapted to selectively apply excess processing power in order to re-process said burst of said input modulated signal.

11. (Original) A demodulator as claimed in claim 10, wherein said first block decoders in said plurality of phase locked loops also generate reliability metric results.

12. (Original) A demodulator as claimed in claim 11, wherein said reliability metric results comprise correlation results taken during decoding by said first block decoders.

13. (Previously Presented) A demodulator as claimed in claim 11, wherein a second block decoder selects codewords from said set of associated codewords based on the reliability metric results from said first block decoders.

14. (Original) A demodulator as recited in claim 10, wherein said selection circuit identifies said burst based on the reliability metric results from said first block decoders.

15. (Original) A demodulator as claimed in claim 14, wherein said demodulator further comprises a second outer block decoder which receives the codewords output from the

first block decoders and selectively corrects errors in the codewords and the selection circuit identifies said burst based on the decoding of the second outer block decoder.

16. (Original) A demodulator as claimed in claim 15, wherein said second block decoder preselects the codewords from among said set of associated codewords.

17. (Original) A demodulator as claimed in claim 16, wherein said preselected codewords comprises the first codewords of the set of associated codewords.

18. (Previously Presented) A communication receiver using a demodulator demodulating an input modulated signal from a transmission channel which is encoded by a sequence of codewords, comprising:

a plurality of phase locked loops which provide respective estimates of the phase of a burst of said input modulated signal, one of said phase locked loops receiving a burst of the input modulated signal and calculating a phase estimate using a different combination of frequency and initial phase estimate and comprising a first block decoder which decodes a set of vector pairs of the burst of said input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate; and

a second block decoder which receives the phase/frequency estimates from said plurality of phase locked loops, wherein one of the bursts is selected based on the decoding of the second block decoder and provided to said one of said plurality of phase locked loops to be re-processed with excess processing power.

19. (Original) A communication receiver as claimed in claim 18, wherein said input modulated signal comprises a phase shift keying modulated signal.

20. (Original) A communication receiver as claimed in claim 18, wherein said first block decoder in each phase locked loop also generates reliability metric results.

21. (Original) A communication receiver as claimed in claim 20, wherein said reliability metric results comprise correlation results taken during decoding by said first block decoders.

22. (Original) A communication receiver as claimed in claim 20, wherein said second block decoder dynamically selects codewords from said set of associated codewords based on the reliability metric results from the corresponding first block decoder.

23. (Original) A communication receiver as claimed in claim 18, wherein said first block decoders are Reed-Muller block decoders.

24. (Original) A communication receiver as claimed in claim 23, wherein said block decoders determine the phase error estimate based on the composite decoded codeword phase error relative to reference.

25. (Original) A communication receiver as claimed in claim 24, wherein said second block decoder preselects the codewords from among said set of associated codewords.

26. (Original) A communication receiver as claimed in claim 25, wherein said preselected codewords comprise the first codewords of the set of associated codewords.

27. (Original) A communication receiver as claimed in claim 19, wherein said down converter down converts said input modulated signal into an intermediate frequency signal, and wherein said communication receiver further comprises:

a synchronous demodulator which demodulates said intermediate frequency signal from a baseband quadrature pair into a sequence of complex sample pairs; and

a matched filter and sampler which passes said sequence of complex sample pairs and samples at a symbol rate to produce said succession of baseband signal samples.

28. (Previously Presented) The demodulator of claim 10, wherein the first block decoder of said one of said plurality of phase locked loops is configured to decode a set of vector pairs of the burst of said input modulated signal at a decode rate to generate the set of associated codewords and the phase/frequency error estimate.

29. (Previously Presented) The demodulator of claim 10, further comprising a second block decoder that receives the phase/frequency estimates from the plurality of phase locked loops, and wherein the selection circuit identifies the burst of the input modulated signal to be demodulated with excess processing power based on the decoding operation of the second block decoder, such that the burst of the input modulated signal to be demodulated with excess processing power is re-processed by said one of said plurality of phase locked loops.

30. (New) The demodulator of claim 10, wherein each of said plurality of phase locked loops is configured to calculate a phase estimate of the bursts of the input modulated signal using a unique combination of frequency and initial phase estimates.

31. (New) The demodulator of claim 30, wherein a quantity of said plurality of phase locked loops is equal to a quantity of possible unique combinations of frequency and initial phase estimates.

32. (New) The demodulator of claim 10, wherein each of said plurality of phase locked loops are configured to process the bursts of the input modulated signal serially.

33. (New) The demodulator of claim 10, wherein each of said plurality of phase locked loops comprises a second decoder, and wherein the selection circuit determines the burst to be re-processed with excess processing power based on a likelihood of phase estimation failure based on the output of the second decoder of each of said plurality of phase locked loops.